AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Previously Amended) A semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate,

wherein a first voltage is applied to said plurality of first MOS transistors,

wherein a second voltage smaller than said first voltage is applied to said plurality of second MOS transistors,

wherein a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a gate length of a second gate electrode of said plurality of second MOS transistors, and

wherein a spacing between said first gate electrode of the first MOS transistors and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a spacing betwe n said second gate electrode and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors.

2. (Previously Amended) A semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate,

wherein a first voltage is applied to said plurality of first MOS transistors,

wherein a second voltage smaller than said first voltage is applied to said plurality of second MOS transistors,

wherein a gate length of a first gate electrode of said plurality of first MOS transistors is larger than a

gate length of a second gate electrode of said plurality of second MOS transistors, and

wherein a spacing between an edge of a first active region in which the first MOS transistors are formed and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a spacing between an edge of a second active region in which the second MOS transistors are formed and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors.

3. (Previously Amended) A semiconductor device according to Claim 1,

wherein said input circuit or said output circuit operates with said first voltage, and

wherein said internal circuit operates with said second voltage.

4. (Previously Amended) A semiconductor device according to Claim 1,

wherein said plurality of first MOS transistors are first voltage withstanding MOS transistors, and

wherein said plurality of second MOS transistors are second voltage withstanding MOS transistors.

5. (Previously Amended) A semiconductor device according to Claim 1,

wherein a gate insulating film thickness of the first MOS transistors is larger than a gate insulating film thickness of the second MOS transistors.

6. (Previously Amended) A semiconductor device according to Claim 1,

wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed.

7. (Previously Amended) A semiconductor device according to Claim 1,

wherein said plurality of first MOS transistors are p-channel type, and the source of each of said plurality of first MOS transistors is supplied with said first voltage, and

wherein said plurality of second MOS transistors are p-channel type, and the source of each of said plurality of second MOS transistors is supplied with said second voltage.

8-20 (Cancelled)

21. (Previously Amended) A semiconductor device according to Claim 2,

wherein said input circuit or said output circuit operates with said first voltage, and wherein said internal circuit operates with said second voltage.

22. (Previously Amended) A semiconductor device according to Claim 2,

wherein said plurality of first MOS transistors are first voltage withstanding MOS transistors, and

wherein said plurality of second MOS transistors are second voltage withstanding MOS transistors.

23. (Previously Amended) A semiconductor device according to Claim 2,

wherein a gate insulating film thickness of the first MOS transistors is larger than a gate insulating film thickness of the second MOS transistors.

24. (Previously Amended) A semiconductor device according to Claim 2,

wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed.

25. (Previously Amended) A semiconductor device according to Claim 2,

wherein said plurality of first MOS transistors are p-channel type, and the source of each of said plurality of first MOS transistors is supplied with said first voltage, and

wherein said plurality of second MOS transistors are p-channel type, and the source of each of said plurality of second MOS transistors is supplied with said second voltage.

26. (Cancell d)